## Introduction

什么是APB?

Advanced Peripheral Bus.

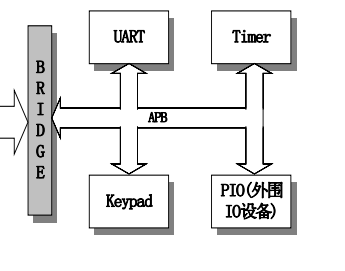
特点：

主要用在低速且低功率消耗的外围。

1. low-cost, low-bandwidth
2. low-complexity
3. All signal transitions are only related to the rising edge of the clock

所有信号必须在时钟上升沿进行传递。使得APB容易整合进大部分的设计流程中。

1. Every transfer takes at least two cycles.
2. 架构简单，只有一个M：APB bridge.



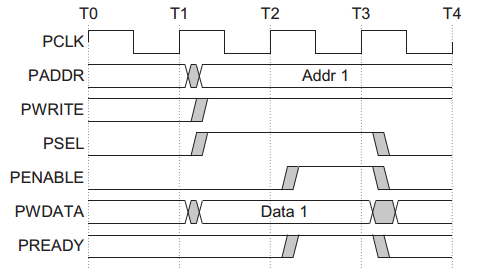
## Transfers

1. **Write transfer:**

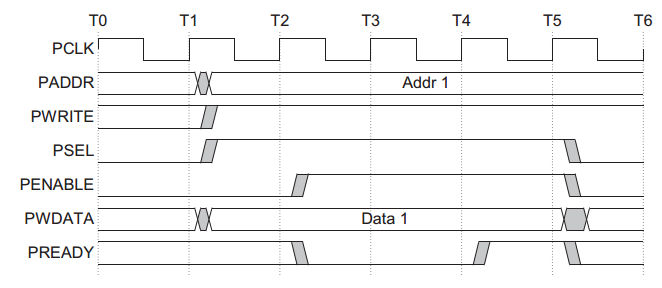
Two types:

* With no wait states
* With wait states

With no wait states:



With wait states:



The **PREADY** signal from the slave can extend the transfer.

The following signals remain unchanged for the additional cycles:

* Address: **PADDR**
* Write signal: **PWRITE**
* Select signal: **PSEL**
* Write data: **PWDATA**

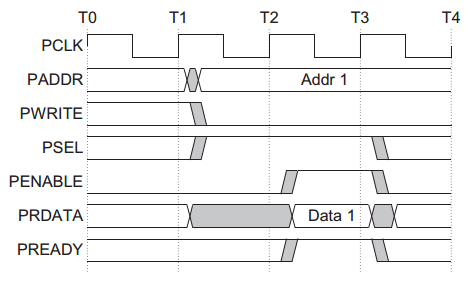
**PREADY** can be any value when **PENABLE** is LOW.

1. **Read transfers**

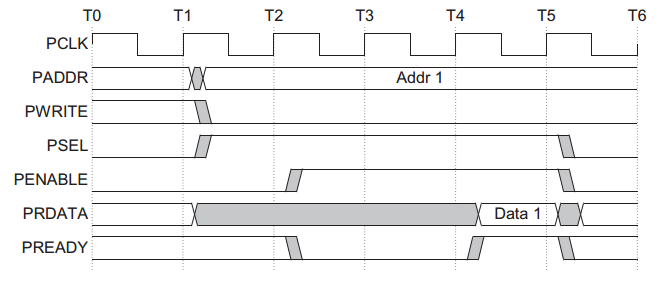
Two types:

* With no wait states
* With wait states

With no wait states:



With wait states:



The **PREADY** signal can extend the transfer.

The protocol ensures that the following remain unchanged for the additional cycles:

* Address: **PADDR**
* Write signal: **PWRITE**
* Select signal: **PSEL**
* Enable signal: **PENABLE**

**PREADY** can be any value when **PENABLE** is LOW.

1. **Error response**

**Write transfer**

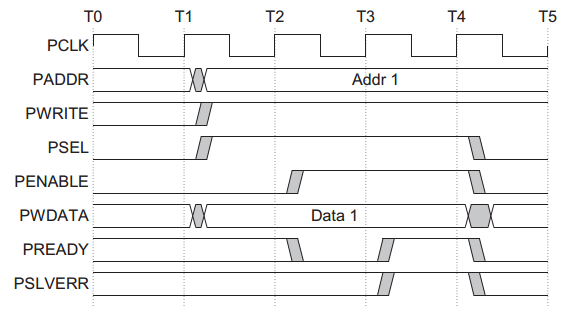


Figure shows an example of a failing write transfer that completes with an error.

**Read transfer**

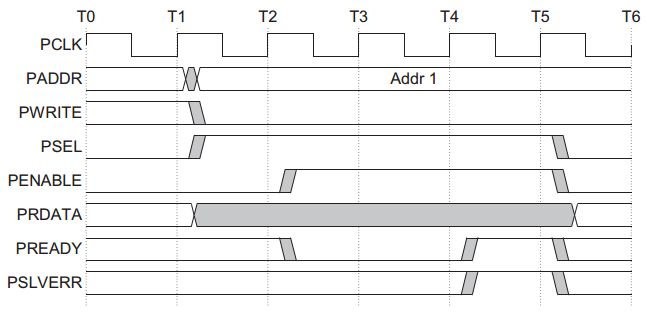
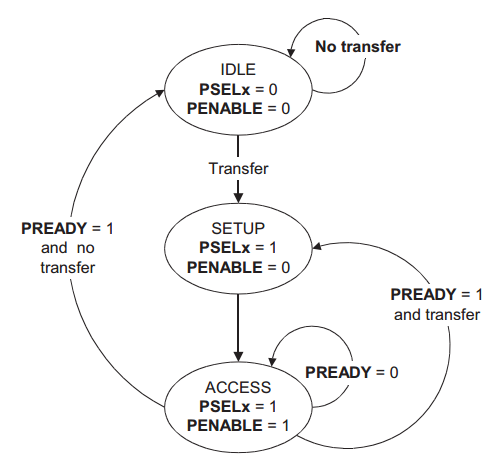


Figure shows a read transfer completing with an error response.

## Operating states



The state machine operates through the following states:

**IDLE** This is the default state of the APB.

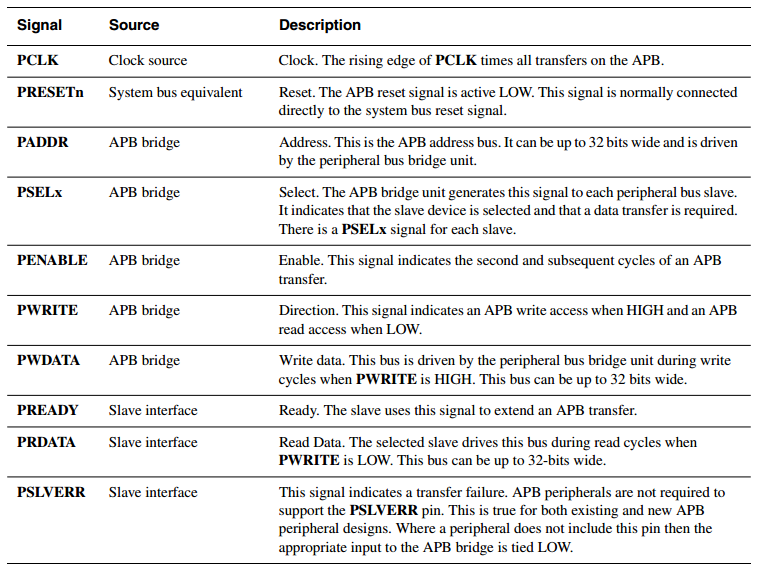
**SETUP** When a transfer is required the bus moves into the SETUP state, where the appropriate select signal, **PSELx**, is asserted. The bus only remains in the SETUP state for one clock cycle and always moves to the ACCESS state on the next rising edge of the clock.

**ACCESS** The enable signal, **PENABLE**, is asserted in the ACCESS state. The address, write, select, and write data signals must remain stable during the transition from the SETUP to ACCESS state.

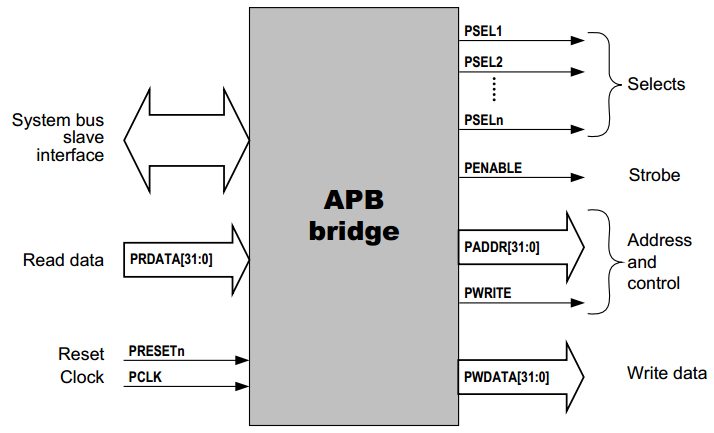
Exit from the ACCESS state is controlled by the **PREADY** signal from the slave:

* If **PREADY** is held LOW by the slave then the peripheral bus remains in the ACCESS state.
* If **PREADY** is driven HIGH by the slave then the ACCESS state is exited and the bus returns to the IDLE state if no more transfers are required. Alternatively, the bus moves directly to the SETUP state if another transfer follows.

## Signal description



## APB Bridge



APB桥将系统总线传送转换成APB方式的传送，它具备一些这些功能：

* 锁存地址，在传送过程中保持地址有效。锁存读写控制信号
* 对锁存的地址进行译码并产生选择信号PSELx，在传送过程中只有一个选择信号可以被激活。也就是选择出唯一 一个APB从设备以进行读写动作.
* 写操作时: 负责将AHB送来的数据送上APB总线。
* 读操作时: 负责将APB的数据送上AHB系统总线。
* 产生一时序选通信号PENABLE来作为数据传递时的启动信号